The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A signal processing system suitable for processing transducer signals in a low power measuring instrument, the signal processing system comprising;

a reference signal generator for generating an ADC ramp signal;

two or more differential signal channels, each differential signal channel comprising:

a first comparator comprising a first input, a second input, and an output, the first input of the first comparator receiving the first signal of a pair of differential signals, the second input of the first comparator receiving the ramp signal, the output of the first comparator providing a first-comparator output signal based on the signals at the first and second inputs; and

a second comparator comprising a first input, a second input, and an output, the first input of the second comparator receiving the second signal of the pair of differential signals, the second input of the second comparator receiving the ramp signal, the output of the second comparator providing a second-comparator output signal based on the signals at the first and second inputs; and

one or more digital differential value determining circuits for receiving the first-comparator output signal and the second-comparator output signal of at least one of the differential signal channels and determining a digital value representative of the difference between the pair of differential signals received by the at least one differential signal channel;

wherein the signal processing system is operable from a low voltage power supply to process the signals of the at least two differential signal channels in parallel and determine the corresponding digital values in parallel.

2. The signal processing system of Claim 1, wherein the signal processing system is operable from a low voltage power supply providing a voltage less than 3.5 volts.

3. The signal processing system of Claim 1, wherein the signal processing system is operable from a low voltage power supply providing a voltage less than 1.75 volts.

4. The signal processing system of Claim 1, wherein the signal processing system is operated from a portable low power low voltage power supply.

5. The signal processing system of Claim 4, wherein the portable low power low voltage power supply comprises at least one of a battery and solar cell.

6. The signal processing system of Claim 5, wherein the battery comprises at least one of a 3 volt coin type battery, a 3 volt button type battery, a 1.5 volt coin type battery, and a 1.5 volt button type battery.

7. The signal processing system of Claim 4, wherein the portable low power low voltage power supply comprises the power supply of a portable measuring instrument which includes the signal processing system, and the portable low power low voltage power supply supplies a total average current of 10 microamps or less to the portable measuring instrument during normal operation.

8. The signal processing system of Claim 1, wherein at least the reference signal generator, the differential signal channels and the digital differential value determining circuit are fabricated on a single silicon substrate in an integrated circuit.

9. The signal processing system of Claim 8, wherein the at least one digital differential value determining circuit comprises at least one clock circuit fabricated entirely on the single silicon substrate in the integrated circuit; the clock circuit configured such that for at least one comparator included in the clock circuit a trip-point voltage of the comparator and a voltage change rate of a clock ramp signal input to the comparator are both controlled based on a common signal, such that variations in a voltage supplied to the clock during normal operation does not substantially affect the clock period.

10. The signal processing system of Claim 9, wherein:

the clock circuit further comprises at least one resistor having a resistance that is a primary determinant of the common signal, and at least one capacitor having a capacitance that is a primary determinant the voltage change rate of the clock ramp signal;

the reference signal generator comprises at least one resistor having a resistance that is a first primary determinant of the generated ADC ramp signal, and at least one capacitor having a capacitance that is a second primary determinant of the generated ADC ramp signal; and

wherein a scale factor of the signal processing circuit is affected mainly by the resistance that is a primary determinant of the common signal, the capacitance that is a primary determinant the voltage change rate of the clock ramp signal, the resistance that is a first primary determinant of the generated ADC ramp signal, the capacitance that is a second primary determinant of the generated ADC ramp signal, and the value of a voltage supplied to the reference signal generator during normal operation.

11. The signal processing system of Claim 10, further comprising a power supply usable to provide a first voltage level to the reference signal generator during normal operation and further usable to provide a second voltage level proportional to the first voltage level to a transducer which determines at least one pair of differential signals received by the signal processing system during normal operation;

wherein the scale factor of the signal processing circuit and the signal amplitude of the differential signals determined by the transducer change proportionately with regard to variations in the voltage of the power supply, such that the overall measurement accuracy of a measuring instrument including the signal processing system and the transducer is substantially insensitive to variations in the voltage of the power supply during normal operation.

12. The signal processing system of Claim 1, wherein the at least one digital differential value determining circuit comprises at least one clock circuit

fabricated on a single silicon substrate in an integrated circuit, the clock controllable to start operation at the start of periods during which the at least one digital differential value determining circuit determines the digital value representative of the difference between the pair of differential signals and to stop operation at the end of such periods.

13. The signal processing system of Claim 1, wherein the at least one digital differential value determining circuit comprises at least one clock circuit operable to output repetitive clock cycles and at least one counter circuit corresponding to each at least one differential channel for counting the repetitive clock cycles;

the digital differential value determining circuit starting a count of the repetitive clock cycles based on the first-comparator output signal of a differential channel; and

the digital differential value determining circuit ending the count of the repetitive clock cycles based on the second-comparator output signal of the differential channel;

wherein the digital value representative of the difference between the pair of differential signals received by that differential channel is based on the count of repetitive clock cycles.

14. The signal processing system of Claim 1, wherein the ADC ramp signal generated by the reference signal generator comprises a linear single ramp reference signal.

15. The signal processing system of Claim 1, wherein at least one pair of differential signals depend on the operation of a transducer included in a low power measuring instrument which also includes the signal processing system, the low power measuring instrument operable to determine a measurement based on the digital values.

16. The signal processing system of Claim 15, wherein the at least two differential signal channels comprise at least three differential signal channels, the transducer comprises a three-phase displacement transducer, and the at least one digital differential value determining circuit determining at least three digital values representative of the differences between at least three pairs of differential signals received by the at least three differential signal channels, the at least three digital values further processable to determine a displacement measurement which is substantially free of at least one of third harmonic spatial distortion and third harmonic signal processing distortion.

17. The signal processing system of Claim 16, wherein the transducer is an inductive displacement transducer of a type such as linear, angular, or rotary.

18. The signal processing system of Claim 17, wherein the low power measuring instrument is a handheld portable measuring instrument.

19. A signal processing system suitable for processing transducer signals in a low power measuring instrument, the signal processing system comprising;

a reference signal generator for generating an ADC ramp signal;

one or more differential signal channels, each differential signal channel comprising:

a first comparator comprising a first input, a second input, and an output, the first input of the first comparator receiving the first signal of a pair of differential signals, the second input of the first comparator receiving the ramp signal, the output of the first comparator providing a first-comparator output signal based on the signals at the first and second inputs; and

a second comparator comprising a first input, a second input, and an output, the first input of the second comparator receiving the second signal of the pair of differential signals, the second input of the second comparator receiving the ramp signal, the output of the second comparator providing a second-comparator output signal based on the signals at the first and second inputs; and

one or more digital differential value determining circuits for receiving the first-comparator output signal and the second-comparator output signal of at least one differential signal channel and determining a digital value representative of the difference between the pair of differential signals received by the at least one differential signal channel; and

wherein the one or more digital differential value determining circuits comprise at least one clock circuit configured such that for at least one comparator included in the clock circuit a trip-point voltage of the comparator and a voltage change rate of a clock ramp signal input to the comparator are both controlled based on a common signal, such that variations in a voltage supplied to the clock during normal operation does not substantially affect the clock period.

20. A signal processing method suitable for processing transducer signals in a low power measuring instrument, the signal processing method comprising;

generating an ADC ramp signal;

for each of at least two differential signal channels;

receiving the first signal of a pair of differential signals at a first input of a first comparator of the differential signal channel and receiving the ramp signal at a second input of the first comparator of the differential signal channel;

outputting a first-comparator output signal based on the signals at the first and second inputs of the first comparator; and

receiving the second signal of a pair of differential signals at a first input of a second comparator of the differential signal channel and receiving the ramp signal at a second input of the second comparator of the differential signal channel;

outputting a second-comparator output signal based on the signals at the first and second inputs of the second comparator; and

determining a digital value representative of the difference between each pair of differential signals received by a differential signal channel based on the first-comparator output signal and the second-comparator output signal of that differential signal channel;

wherein the generating, receiving, outputting and determining steps are performed to determine the digital values corresponding to each differential channel in parallel, and

wherein the generating, receiving, outputting and determining steps are performed using voltage signals which do not exceed 3.5 volts.

21. The signal processing method of Claim 20, wherein the generating, receiving, outputting and determining steps are performed using voltage signals which do not exceed 1.75 volts.

22. The signal processing method of Claim 20, wherein the signal processing method further comprises repeating the generating, receiving, outputting and determining steps as part of the operation of a measuring instrument which is operated from a portable low power low voltage power supply.

23. The signal processing method of Claim 22, wherein the generating, receiving, outputting and determining steps are performed using voltage signals which do not exceed the voltage provided by the portable low power low voltage power supply.

24. The signal processing method of Claim 22, wherein the portable low power low voltage power supply comprises at least one of a battery and a solar cell.

25. The signal processing method of Claim 24, wherein the battery comprises at least one of a 3 volt coin type battery, a 3 volt button type battery, a 1.5 volt coin type battery, and a 1.5 volt button type battery.

26. The signal processing method of Claim 22, wherein the portable low power low voltage power supply supplies a total average current of 10 microamps or less to the portable measuring instrument during normal operation.

27. The signal processing method of Claim 20, further comprising generating at least one clock signal based on the operation of at least one comparator

wherein a trip-point voltage of the comparator and a voltage change rate of a clock ramp signal input to the comparator are both controlled based on a common signal such that normal variations in a voltage supply used to generate the clock signal do not substantially affect the clock period and wherein the clock signal is used in the step of determining a digital value.

28. The signal processing method of Claim 27, further comprising:

providing a first voltage used to generate the ADC ramp signal;

providing a second voltage proportional to the first voltage to a transducer which determines at least one pair of differential signals received by a corresponding differential signal channel;

wherein a scale factor associated with the signal processing method and the signal amplitude of the differential signals determined by the transducer change proportionately with regard to proportional variations in the first and second voltages, such that for a measuring instrument including the transducer and which also includes the signal processing method as part of the operation of the measuring instrument the overall measurement accuracy of the measuring instrument is substantially insensitive to normal variations in a power supply used to provide the first and second voltages.

29. The signal processing method of Claim 20, wherein the step of determining a digital value representative of the difference between each pair of differential signals received by a differential signal channel comprises starting a clock signal at the start of periods during which a digital value representative of the difference between a pair of differential signals received by a differential signal channel is being determined and stopping the clock signal at the end of such periods.

30. The signal processing method of Claim 20, the method further comprising generating repetitive clock cycles, and wherein the step of determining a digital value representative of the difference between each pair of differential signals received by a differential signal channel comprises:

starting a count of the repetitive clock cycles based on the first-comparator output signal of a differential channel; and

ending the count of the repetitive clock cycles based on the second-comparator output signal of the differential channel; and

determining the digital value representative of the difference between the pair of differential signals received by the differential channel based on the count of repetitive clock cycles.

31. The signal processing method of Claim 20, wherein the step of generating an ADC ramp comprises generating a linear single ramp signal.

32. The signal processing method of Claim 20, wherein at least one pair of received differential signals depend on the operation of a transducer included in a low power measuring instrument which also includes the signal processing method as part of the operation of the measuring instrument, the low power measuring instrument operable to determine a measurement based on the digital values.

33. The signal processing method of Claim 32, the at least two differential signal channels comprising at least three differential signal channels and the transducer comprising a three-phase displacement transducer, wherein the step of determining a digital value representative of the difference between each pair of differential signals received by a differential signal channel comprises determining at least three digital values representative of the differences between at least three pairs of differential signals received by the at least three differential signal channels, the at least three digital values further processable to determine a displacement measurement which is substantially free of at least one of third harmonic spatial distortion and third harmonic signal processing distortion.

34. The signal processing method of Claim 33, wherein the transducer is an inductive displacement transducer of a type such as linear, angular, or rotary.

35. The signal processing method of Claim 34, wherein the low power measuring instrument is one of a portable measuring instrument and a handheld portable measuring instrument.

36. A signal processing method suitable for processing transducer signals in a low power measuring instrument, the signal processing method comprising;

generating an ADC ramp signal;

for at least one differential signal channel;

receiving the first signal of a pair of differential signals at a first input of a first comparator of the differential signal channel and receiving the ramp signal at a second input of the first comparator of the differential signal channel;

outputting a first-comparator output signal based on the signals at the first and second inputs; and

receiving the second signal of a pair of differential signals at a first input of a second comparator of the differential signal channel and receiving the ramp signal at a second input of the second comparator of the differential signal channel;

outputting a second-comparator output signal based on the signals at the first and second inputs;

generating at least one clock signal based on the operation of at least one comparator wherein a trip-point voltage of the comparator and a voltage change rate of a clock ramp signal input to the comparator are both controlled based on a common signal such that normal variations in a voltage supply used to generate the clock signal do not substantially affect the clock period and wherein the clock signal is used in the step of determining a digital value; and

determining a digital value representative of the difference between each pair of differential signals received by a differential signal channel based on the first-comparator output signal and the second-comparator output signal of that differential signal channel and the generated at least one clock signal.